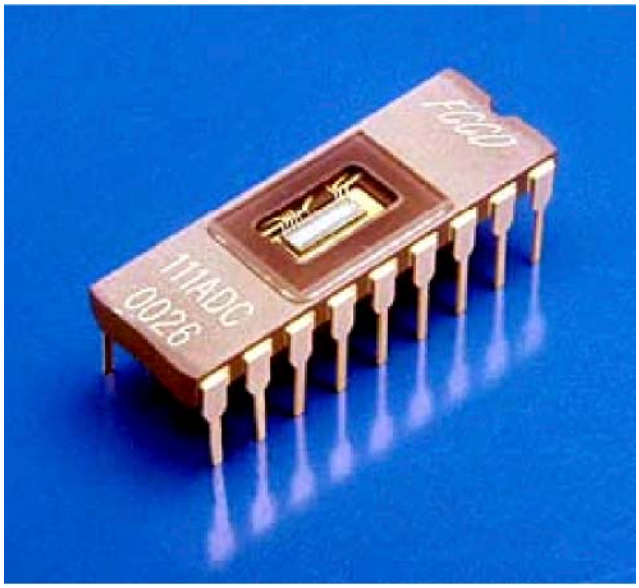
CCD 111
256-Element
Line Scan Image Sensor

FEATURES

- **256 x 1 photosite array**
- **13µm x 17µm photosites on 13µm pitch**
- **Dynamic range typical: 7000:1**
- **On-chip video and compensation amplifiers**
- **Low power requirements**
- **All operating voltages 15V and under**
- **Low noise equivalent exposure**
- **Dimensionally precise photosite spacing**
- **RoHS Compliant**



GENERAL DESCRIPTION

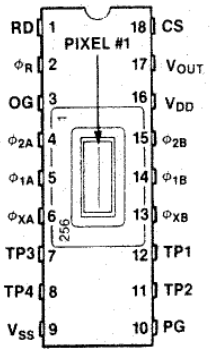
The CCD111 is a monolithic 256-element line image sensor. The device is designed for optical character recognition and other imaging applications that require high sensitivity and high speed. The CCD111 is pin-for-pin compatible with and a functional replacement for the CCD110F.

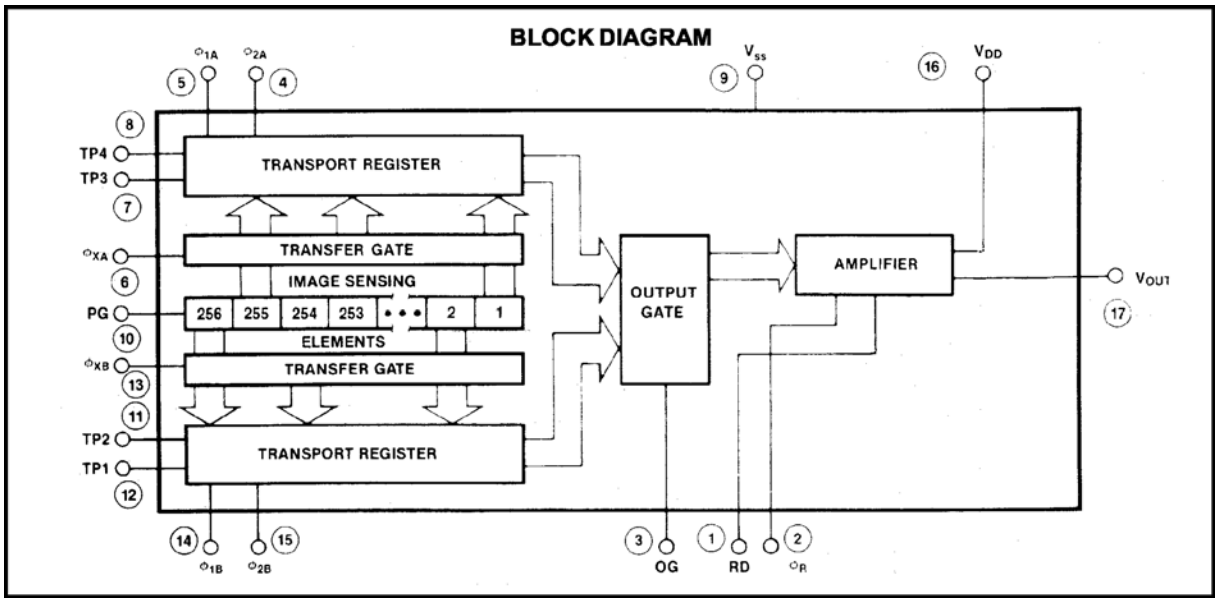
In addition to a line of 256 sensing elements, the CCD111 chip includes two charge transfer gates, two 2-phase analog transport shift registers, an output charge detector/amplifier, and a compensation amplifier. The transport registers both feed the input of the charge detector resulting in sequential reading of the 256 sensing elements.

The cell size is 13µm (0.51 mils) by 17µm (0.67 mils) on 13µm (0.51 mils) centers. The device is manufactured using Fairchild Imaging advanced CCD n-channel isoplanar buried-channel technology.

PIN NAME	DESCRIPTION
PG	Photogate
ϕXA, ϕXB	Transfer Clocks
ϕ1A, ϕ2A	Transport Clocks
ϕ1B, ϕ2B	
OG	Output Gate
V_{OUT}	Output Source
V_{DD}	Output Drain
CS	Compensation Source
ϕR	Reset Clock
RD	Reset Drain
TP	Test Point
V_{SS}	Substrate (ground)

PIN CONNECTION DIAGRAM (TOP VIEW)





FUNCTIONAL DESCRIPTION

The CCD111 consists of the following functional elements illustrated in the Block Diagram.

Image Sensor Elements – A row of 256 image sensor elements separated by a diffused channel stop and covered by a silicon photogate. Image photons pass through the transparent polycrystalline silicon photogate and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated background level at zero illumination to a maximum at saturation under bright illumination.

Two Transfer Gates – Gate structures adjacent to the row of image sensor elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers whenever the transfer gate voltages go High. Alternate charge packets are transferred to the left and right transport registers. The transfer gates also control the integration time for the sensing elements.

Two 130-bit Analog Transport Shift Registers – One on each side of the line of image sensor elements and separated from it by a transfer gate. The two registers, called the transport registers, are used to move the light generated charge packets delivered by the transfer gates serially to the charge detector/amplifier. The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge packets to establish the original serial sequence of the line of video in the output circuit.

A Gated Charge Detector/Amplifier – Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of the output n-channel MOS transistor producing a signal at the output OS. A reset transistor is driven by the reset clock (R) and recharges the charge detector diode capacitance before the arrival of each new signal charge packet from the transport resisters

DEFINITION OF TERMS

Charge-Coupled Device – A charge-coupled device is a semiconductor device in which finite isolated charge packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge packets are minority carriers with respect to the semiconductor substrate.

Transfer Clocks XA, XB – The voltage waveforms applied to the transfer gates to move the accumulated charge from the image sensor elements to the CCD transport registers.

Transport Clocks 1A, 2A, 1B, 2B – The two sets of 2-phase waveforms applied to the gates of the transport registers to move the charge packets received from the image sensor elements to the gated charge detector/ amplifier.

Gated Charge Detector/Amplifier – The output circuit of the CCD111 that receives the charge packets from the transport registers and provides a signal voltage proportional to the size of each charge packet received. Before each new charge packet is sensed, a reset clock returns the charge detector voltage to a fixed level.

Reset Clock R – The voltage waveform required to reset the voltage on the charge detector.

Dynamic Range – The saturation exposure divided by the rms noise equivalent exposure (this does not take into account dark signal components). Dynamic range is sometimes defined in terms of peak-to-peak noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

RMS Noise Equivalent Exposure – The exposure level that gives an output signal equal to the rms noise level at the output in the dark.

Saturation Exposure — The minimum exposure level that will produce a saturation output signal. Exposure is equal to the irradiance times the photosite integration time.

Charge Transfer Efficiency — Percentage of valid charge information that is transferred between each successive stage of the transport registers.

Responsivity — The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure.

Total Photoresponse Non-uniformity — The difference of the response levels of the most and least sensitive element under uniform illumination. Measurement of PRNU excludes first and last elements. (See accompanying photos for details of definition.)

Dark Signal — The output signal in the dark caused by thermally generated electrons that is a linear function of the integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

Saturation Output Voltage — The maximum usable signal output voltage. Charge transfer efficiency decreases sharply when the saturation output voltage is exceeded.

Integration Time — The time interval between the falling edges of any two transfer pulses ØXA or ØXB as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel — A picture element (photosite).

Peripheral Response — The output signal caused by light-generated charge that is collected by the transport registers (instead of the photosites). The primary cause of peripheral response on CCD111A/B devices manufactured after date code 81-01 is optical crosstalk from the photosites to the shift registers.

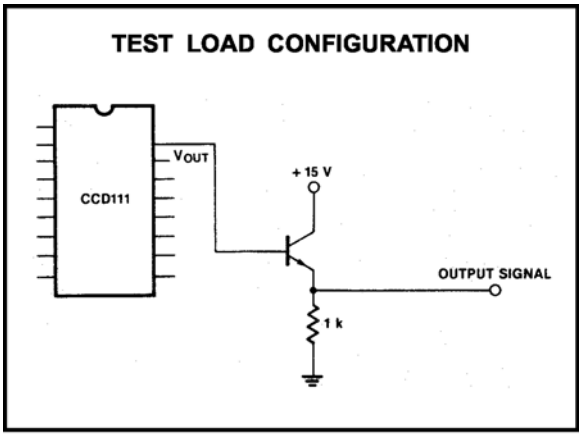
Major Differences Between the CCD111A and CCD111B - Both the CCD111A and the CCD111B have the same responsivity to visible light (400-700nm). The peripheral differences are as follows:

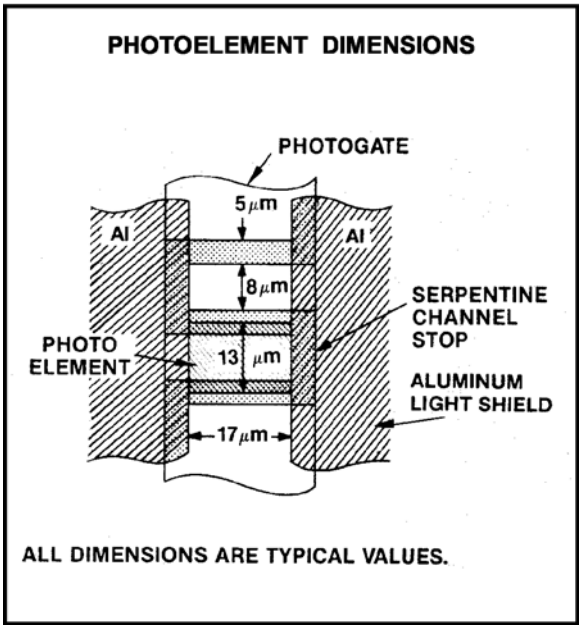
- The CCD111A is intended for use in applications where very dark signal and high responsivity to very near-infrared (700-900nm) light are needed, and where peripheral response is not critical.
- The CCD111B is selected for use in applications where standard responsivity to very near-infrared (700-900nm) light and standard dark signal are acceptable and where peripheral response needs to be minimized.
- It is not recommended that either part be used with illumination containing wavelengths greater that 900nm (nearinfrared). If use of such a light source (unfiltered tungsten, for example) is unavoidable, the CCD111B will generally provide the user with more satisfactory results. The table on performance characteristics provides more information.

Absolute Maximum Ratings

Storage Temperature: -25° C to 100° C
Operating Temperature: - 25° C to 55° C
Pins 2, 3, 4, 5, 6, 7, 10, 12, 13, 14, 15: -0.3V to 15V
Pins 1, 8, 11, 16: -0.3V to 18V
Pins 17, 18: output, no voltage applied
Pin 9: 0V

Caution Note:
This device has limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins V_{OUT} to V_{SS} or V_{DD} during operation of the device. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.





DC CHARACTERISTICS: T_c = 25°C (Note 1)

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	CONDITION
V_{DD}	Output Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{RD}	Reset Transistor Drain Voltage	11.5	12.0	12.5	V	
V_{OG}	Output Gate Voltage		5.0		V	
V_{PG}	Photogate Voltage	9.5	10.0	12.5	V	
TP1, TP3	Test Points		0.0		V	
TP2, TP4	Test Points	14.5	15.0	15.5	V	

CLOCK CHARACTERISTICS: T_c = 25°C (Note 1)

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	CONDITION
$V\phi_{1AL}$, $V\phi_{1BL}$ $V\phi_{2AL}$, $V\phi_{2BL}$	Transport Clocks LOW	0.0	0.5	0.8	V	Note 2
$V\phi_{1AH}$, $V\phi_{1BH}$ $V\phi_{2AH}$, $V\phi_{2BH}$	Transport Clocks HIGH	7.5	8.0	10.5	V	Note 5
$V\phi_{XAL}$, $V\phi_{XBL}$	Transfer Clock LOW	0.0	0.5	0.8	V	Notes 2, 5
$V\phi_{XAH}$, $V\phi_{XBH}$	Transfer Clock HIGH	7.5	8.0	10.5	V	Note 5
$V\phi_{RL}$	Reset Clock LOW	0.0	0.5	0.8	V	Notes 2, 5
$V\phi_{RH}$	Reset Clock HIGH	9.5	10.0	10.5	V	Notes 3, 5
$f\phi_{1A}$, $f\phi_{1B}$ $f\phi_{2A}$, $f\phi_{2B}$	Maximum Transport Clock Frequency		5.0		MHz	Note 5
$f\phi_R$	Maximum Reset Clock Frequency (Output Data Rate)		10.0		MHz	Note 6

AC CHARACTERISTICS: T_p = 25°C, (Note 1) F_{data}= 1.0MHz, t_{int} = 320ms, $t_{readout}$ = 259ms, Light Source = 285k + 2.0mm thick Schott BG-38 + OCLI WBHM filters. All operating voltages at nominal specified values, All tests done using "Test Load Conditions."

SYMBOL	CHARACTERISTIC	RANGE MIN	RANGE TYP	RANGE MAX	UNIT	CONDITION
DR	Dynamic Range					
	(relative to rms noise)		7000:1			Note 7
	(relative to peak-to-peak noise)		1400:1			
NEE	RMS Noise Equivalent Exposure (A)		0.00008		$\mu J/cm^2$	
	(B)		0.00009		$\mu J/cm^2$	
SE	Saturation Exposure (A)		0.54		$\mu J/cm^2$	
	(B)		0.64		$\mu J/cm^2$	
CTE	Charge Transfer Efficiency	.99990	.99999			Note 8
P	Power Dissipation		100		mW	V_{DD} = 15V
Z	Output Impedance		1		kΩ	
N	RMS Noise		0.1		mV	
	Peak-to-Peak Noise		0.5		mV	

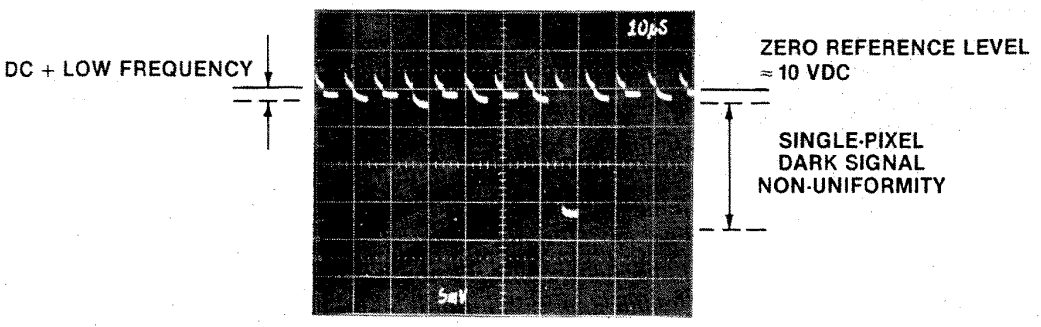
PERFORMANCE CHARACTERISTICS: T_D = 25°C, (Note 1) ,F_{data}= 1.0MHz, t_{int} = 320ms, $t_{readout}$ = 259ms, Light Source = 285k + 2.0mm thick Schott BG-38 + OCLI WBHM filters. All operating voltages at nominal specified values, All tests done using "Test Load Conditions."

		RANGE							
		CCD111A			CCD111B				
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	CONDITION
PRNU	Photoresponse Non-uniformity Peak-to-Peak								
	2854°K with test filters		60	120		70	110	mV	15, 16
	2854° K unfiltered		120			100		mV	15, 16
	Single-pixel Positive Pulses		≤17			≤17		mV	16
	Single-pixel Negative Pulses		35	100		35	100	mV	15, 16
RI	AC Mismatch		≤10			≤10		mV	15, 16
DS	Dark Signal DC Component	0	<1	3	0	2	15	mV	2, 9, 10
	Low Frequency Component	0	<1	2	0	2	10	mV	2, 9, 11
SPDSNU	Single-pixel DS Non-uniformity	0	<1	2	0	1	2	mV	9, 11, 12
PR	Peripheral Response								
	2854° K with test filters		10	17		≤2	5	% of V_{OUT}	14
	2854° K unfiltered		25			4		% of V_{OUT}	14
R	Responsivity								
	2854° K with test filters	1.1	2.0	3.2	0.7	1.3	2.1	V/μJ/cm^2	13, 14
	2854° K unfiltered	2.0	3.6	5.9	1.3	2.4	3.9	V/μJ/cm^2	13, 14
V_{SAT}	Saturation Output Voltage	0.7	1.1	2.0	0.7	1.1	2.0	V	17

NOTES:

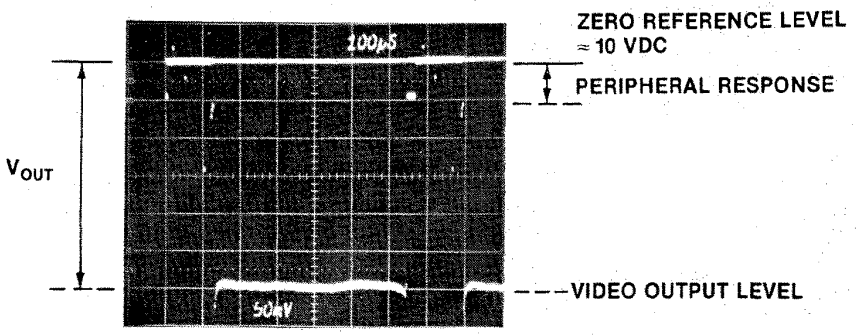
1. T_C is defined as the package temperature, measured on the back surface of the ceramic header.
2. Negative transients on any clock pin going below 0.0V may cause charge injection that results in an increase in the apparent Dark Signal.
3. $V_{\phi RH}$ should track V_{RD}.
4. The data output frequency $f_{\phi R}$ is twice that of each transport clock ($f_{\phi 1A}$, $f_{\phi 1B}$, $f_{\phi 2A}$, $f_{\phi 2B}$).
5. $C_{\phi XA} \simeq C_{\phi XB} \simeq$ 20pF, $C_{\phi 1A} \simeq C_{\phi 2A} \simeq C_{\phi 1B} \simeq C_{\phi 2B} \simeq$ 32pF, $C_{\phi R} \simeq$ 5pF.
6. Minimum reset clock frequency is limited by the increase in Dark Signal.
7. Dynamic Range is defined as "V_{SAT}/rms (temporal) Noise" or "V_{SAT}/Peak-to-Peak (temporal) Noise."
8. CTE is measured for one-stage transfer.
9. See photographs for Dark Signal definitions.
10. DC and low-frequency Dark Signal components approximately double for every 5°C incerase in T_C. The shift register component is also inversely proportional to $f_{\phi R}$.
11. Single-pixel Dark Signal non-uniformity (SPDSNU) approximately doubles for every 8°C increase in T_C. They are also directly proportional to the integration time t_{int}.
12. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU.
13. RESPONSIVITY is defined as the "volts of video output" per "Incident Radiant Energy measured over the 350 nm - 1200 nm band." The device will not respond to infrared wavelengths longer than ≈ 1200 nm. However, 2/3 of the radiant energy from a 2854° K source is at λ > 1200 nm. For the unfiltered 2854° K source, the responsivity values for light measured over 0 < λ < ∞ will be ~0.3X of the responsivity values for light measured over 350 nm < λ < 1200 nm.
14. OPTICAL FILTERS Transmittance curves for filtered and unfiltered light sources are given in the "Typical Performance Curves" section of this data sheet. It should be noted that the filtered source is a good approximation to a Daylight Fluorescent bulb.
15. All PRNU measurements taken at a 600mV output level using a F/5.0 lens; all PRNU measurements exclude the outputs from the first and last photoelements of the array. The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As f number increases, the resulting more highly collimated light causes package window imperfections to dominate and increase the PRNU. A lower f number (f ≤ 5) results in less collimated light, causing photosite blemishes to dominate PRNU.
16. See photographs for PRNU definitions.
17. See test load configuration.

SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITY



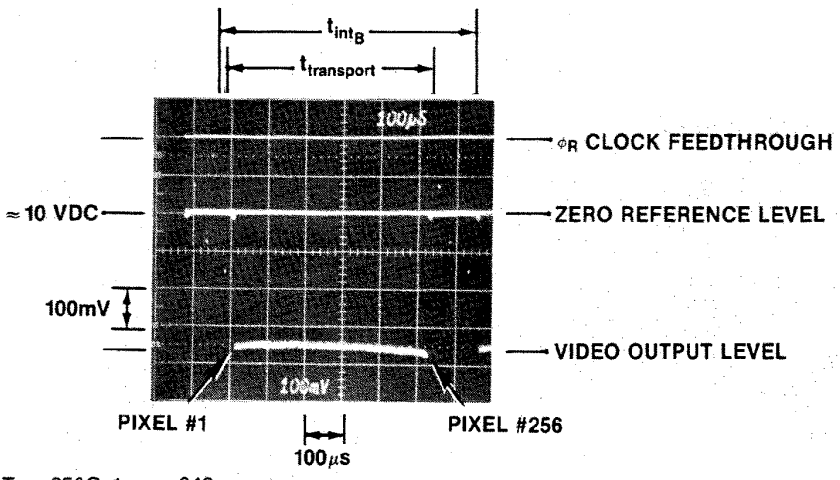
TEST CONDITIONS: T_C = +25° C, t_{int} = 2.560ms, $f_{\phi R}$ = 128 kHz, "typ" voltage inputs. (One-eight standard test speeds to emphasize Dark Signal.)

PERIPHERAL RESPONSE



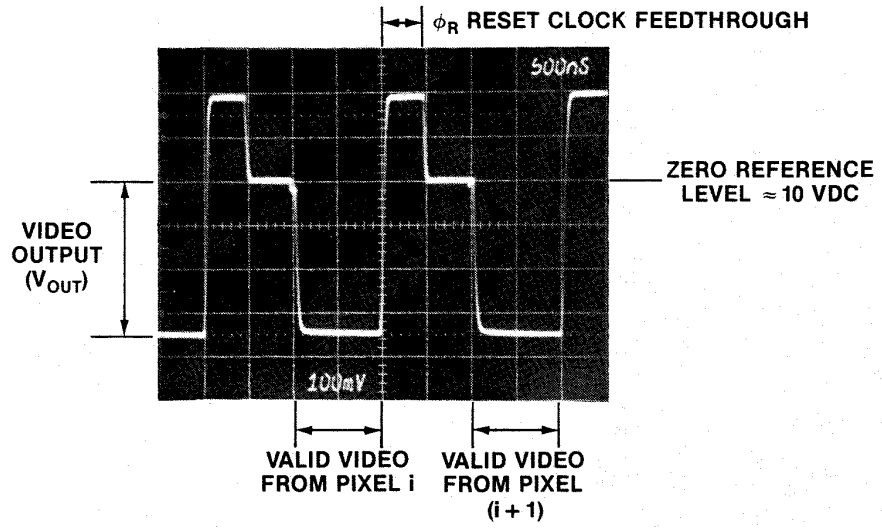
TEST CONDITIONS: T_C = +25° C, t_{int} = 640 μs, $f_{\phi R}$ = 510 kHz, "typ" voltage inputs, 2854° K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

OUTPUT WITH UNIFORM ILLUMINATION

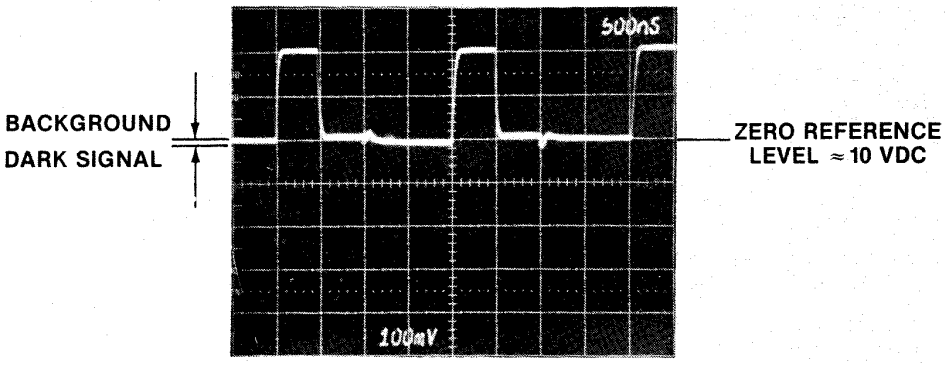


TEST CONDITIONS: T_C + 25°C, t_{int} = 640 μs, f_ϕ = 512 kHz, "typ" voltage inputs, 2854° K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

DEVICE ILLUMINATED

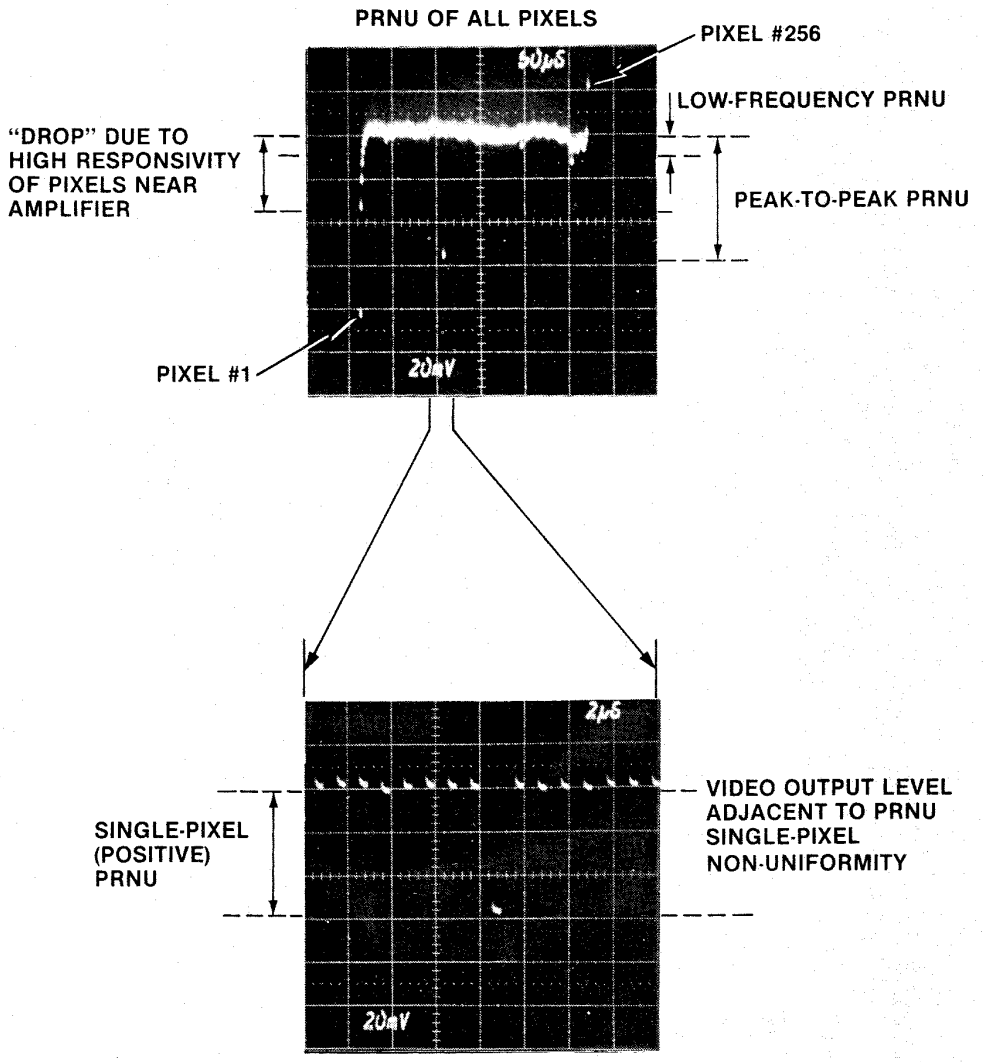


DEVICE IN DARK



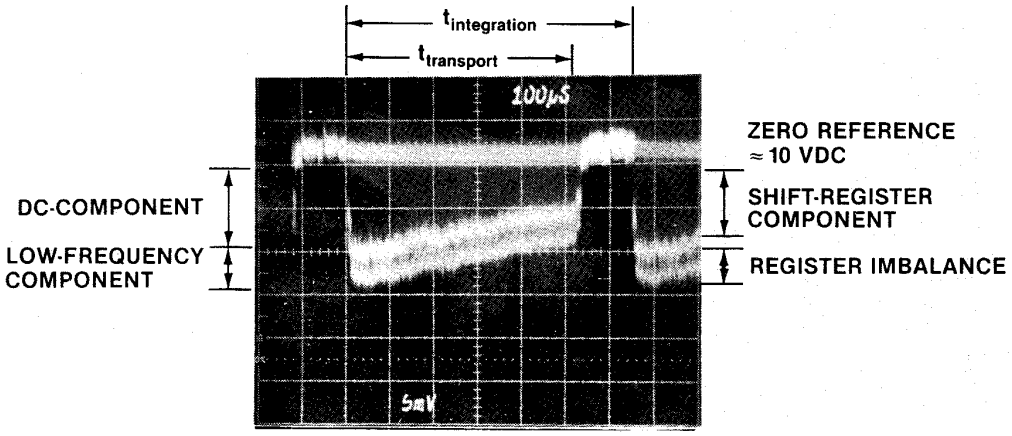
TEST CONDITIONS: T_C + 25°C, t_{int} = 640 μs, f_ϕ = 512 kHz, "typ" voltage inputs, 2854°K + 700 nm cutoff filter set. (Half standard test speeds for clearer photos.)

MEASURED AT V_{OUT} = 350 mV; ALL PRNU COMPONENTS EXCLUDE PIXELS #1 AND #256.

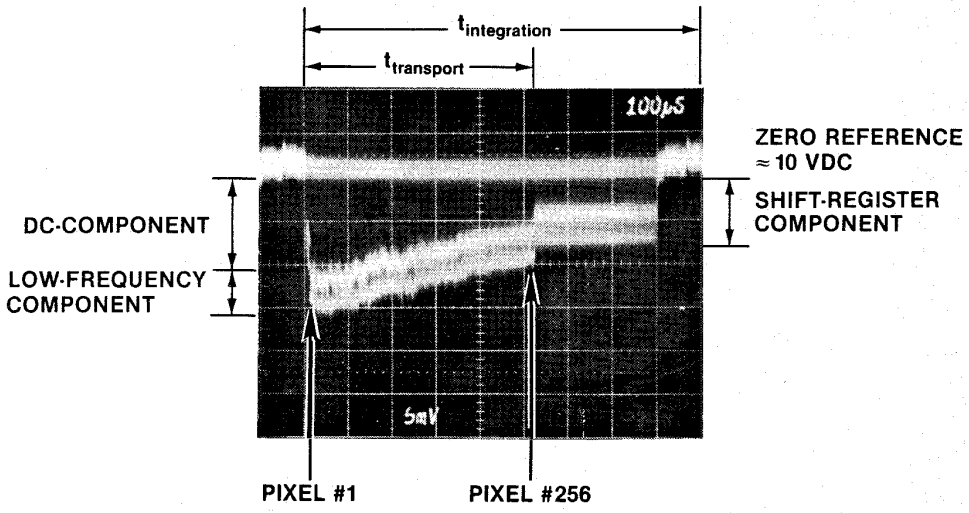


TEST CONDITIONS: T_C = +25°C, t_{int} = 320 μs, $f_{\phi R}$ = 1.0 MHz, 2854°K + 700 nm cutoff filter set, "typ" voltage inputs.

AT t_{int} = 640μs:



AT t_{int} = 900μs, OTHER INPUTS SAME AS ABOVE:



TEST CONDITIONS: T_C = +25°C, t_{int} = (as above), $f_{\phi R}$ = 512 kHz, "typ" voltage inputs, (Half standard test speeds for clearer photos.)

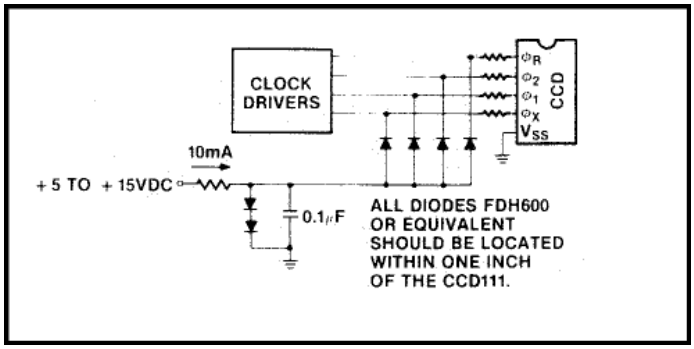
DEVICE CARE AND OPERATION

Charge Injection: Every input pin has a gate protection structure that includes a diode from the input to the (grounded) substrate V_{SS}. The diode is reverse-biased during normal operation ($V_{IN} < V_{SS}$). Negative (transient) input voltages ($V_{IN} < V_{SS}$) will forward-bias the diode, injecting electrons into the bulk silicon of the CCD chip.

If sufficient charge is injected, it will accumulate in the transport register(s) and/or the photosites near the injecting gate protection structure(s). Injected charge which accumulates in the photosites will typically result in apparent bell-shaped increases in Dark Signal (20-200 pixels wide) near the injecting gate protection structure. Injected charge which accumulates in a transport register will result in an apparent uniform increase in that register's low frequency dark signal, creating a noticeable increase in the apparent Register Imbalance ("odd/even") of the Dark Signal.

The susceptibility to charge injection sufficient to increase the DC and Low Frequency Dark Signal varies significantly from device to device. It is not possible to select devices with "low" susceptibility. However, devices with low Dark Signal are typically more susceptible than devices with high Dark Signal.

Sufficient charge to appear as increased DC and Low Frequency Dark Signal may be injected by negative transient voltage < 4 ns long. Since these transients cannot be detected by oscilloscopes with less than 250-500 MHz bandwidth, a system which appears to be free from negative transients on a 200 MHz scope may still be prone to charge injection. The recommended method to eliminate charge injection is the following diode clipper circuit with suitable damping resistors between the clock drivers and the CCD111:

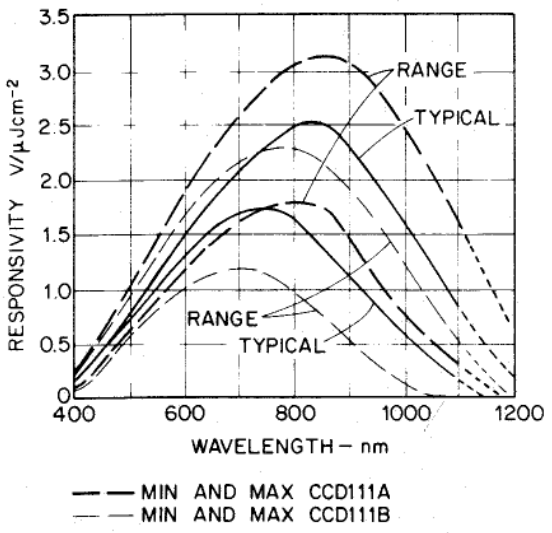


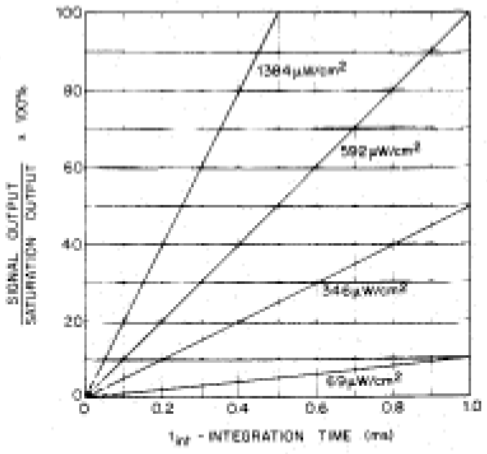
Since $C_R << C_1 = C_1 = (3 \cdot C_X)$, the damping resistors should be selected so that $R_R >> R_1 = R_2 = (1/3 \cdot R_X)$.

It is also important to note in design and application considerations that the devices are very sensitive to thermal conditions. The DC and Low Frequency Dark Signal approximately doubles for every 5°C temperature increase and Dark Signal Non-Uniformities approximately double for every 8°C increase. The devices may be cooled to achieve very long integration times and very low light level capability.

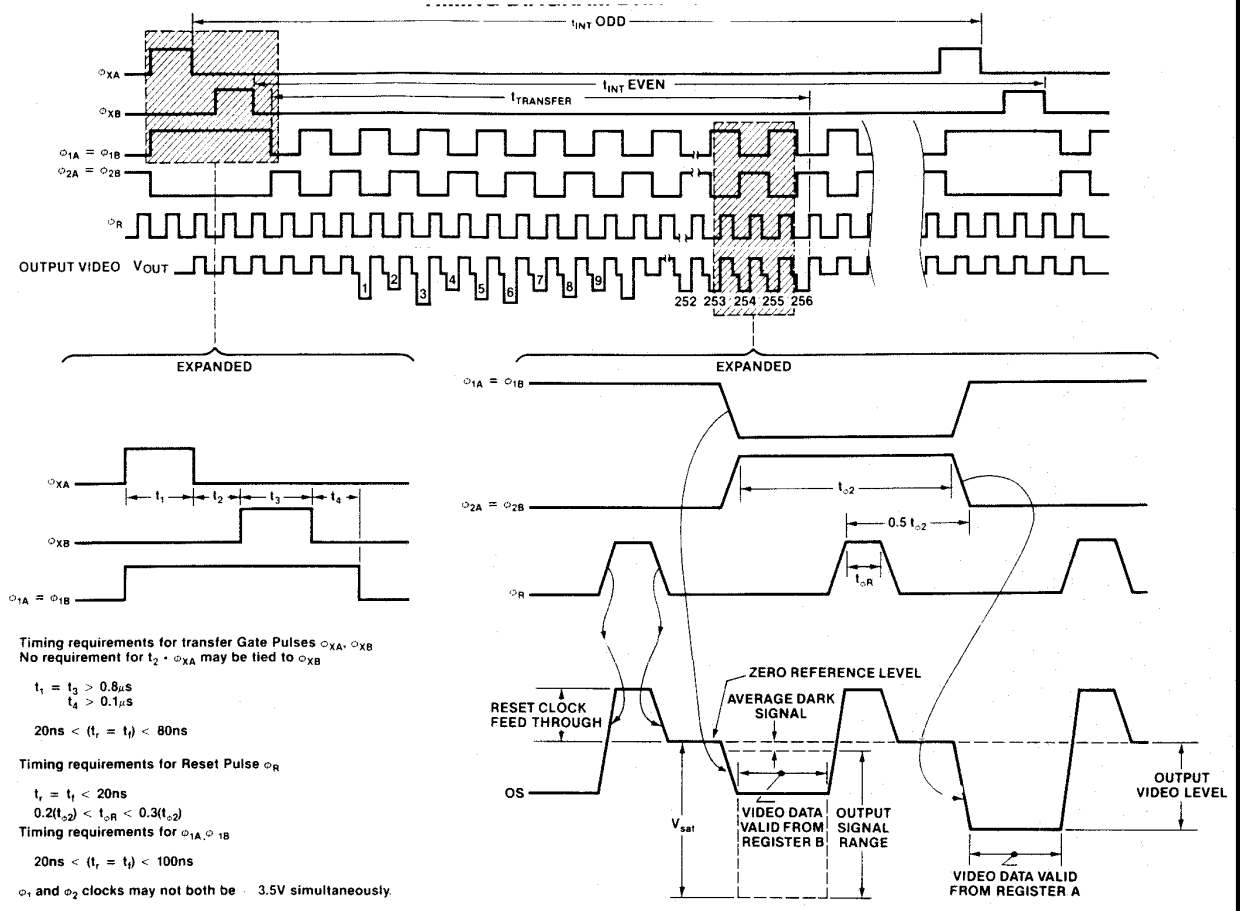
Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

TYPICAL PERFORMANCE CURVES





TIMING DIAGRAM DRIVE SIGNALS



Timing requirements for transfer Gate Pulses ϕ_{XA}, ϕ_{XB}
No requirement for t_2 - ϕ_{XA} may be tied to ϕ_{XB}

$t_1 = t_3 > 0.8\mu s$
$t_4 > 0.1\mu s$

$20ns < (t_r = t_f) < 80ns$

Timing requirements for Reset Pulse ϕ_R

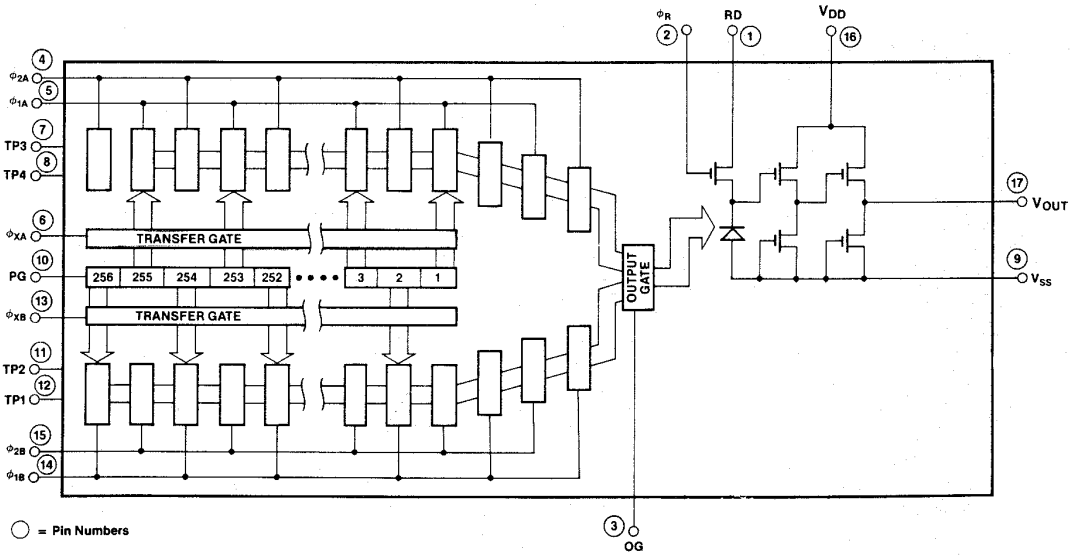
$t_r = t_f < 20ns$
$0.2(t_{\phi 2}) < t_{\phi R} < 0.3(t_{\phi 2})$

Timing requirements for ϕ_{1A}, ϕ_{1B}

$20ns < (t_r = t_f) < 100ns$

ϕ_1 and ϕ_2 clocks may not both be 3.5V simultaneously.

CIRCUIT DIAGRAM



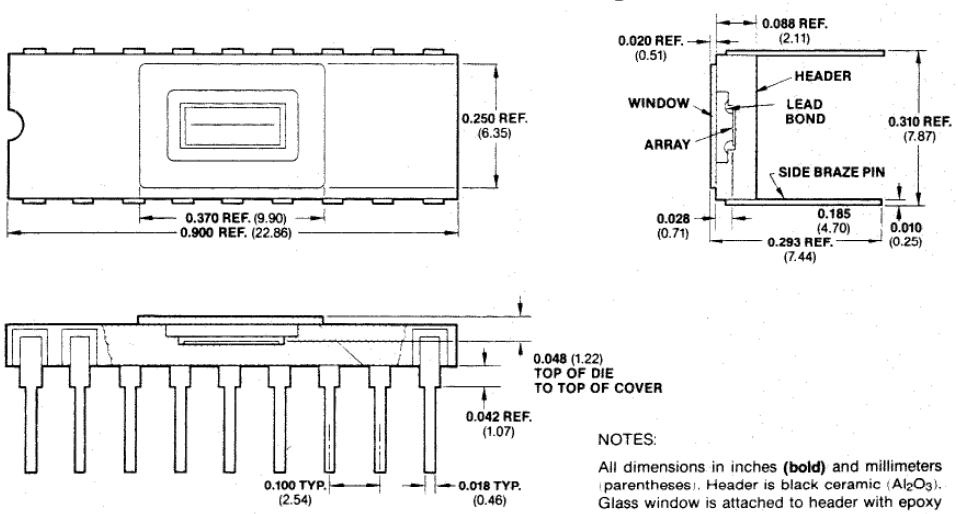
ORDER INFORMATION

It is important to note that two different selections of the CCD111 are being offered for applications that differ in the wavelength of light used for imaging. Please refer to the section "Major Differences Between the CCD111A and CCD111B" on Page 3 before placing an order.

To order the CCD111, please follow the ordering codes listed in the table below.

Description	Device Type Order Code
CCD111A 256 x 1 line image sensor	CCD111ADC
CCD111B 256 x 1 line image sensor	CCD111BDC

CCD111DC Package Outline
24-Pin Dual In-Line Ceramic Package



NOTES:
All dimensions in inches **(bold)** and millimeters (parentheses). Header is black ceramic (Al_2O_3). Glass window is attached to header with epoxy cement. Photosite #1 is located towards the notched end of the package. Terminal #9 is electronically connected to the Substrate (V_{SS}).

WARRANTY

Within twelve months of delivery to the end customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging camera product if any part is found to be defective in materials or workmanship. Contact factory for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Fairchild Imaging certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specification under which it is furnished.

This product is designed, manufactured, and distributed utilizing the ISO 9000:2000 Business Management System.